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An improved transient performance boost converter using pseudo-current hysteresis control

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ABSTRACT

This paper introduces an enhanced low transient voltage and fast transient response boost converter. It uses a hysteresis-controlled circuit fed by a voltage signal from a rail-to-rail current sensor, resulting in improved efficiency, and transient response. The converter is designed using Taiwan semiconductor manufacturing company (TSMC) 0.18 µm CMOS 1P6M technology, delivers an output voltage of 1.8 V while operating with an input voltage range of 0.5 V to 1 V and supports an output load current range of 10 to 100 mA. The key contributions of this paper are: i) introducing a new boost converter architecture employing pseudo-current hysteresis-controlled (PCHC) techniques, ii) incorporating voltage and current loops into the proposed architecture, and iii) demonstrating superior transient performance. Experimental measurements reveal a peak power efficiency of 98.6% at 10 mA and transient times of 15.4 µs and 11.8 µs for a step load change from 10 to 100 mA and back to 10 mA, respectively, with transient voltages of 51 mV. The presented boost converter outperforms in terms of performance, compared to previous works using the figure of merit (FOM) formula.

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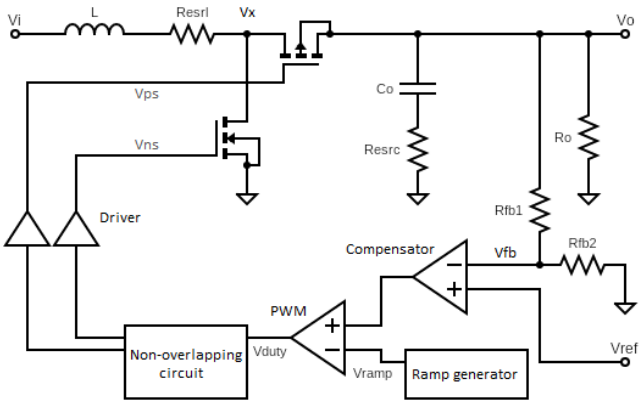
1. INTRODUCTION

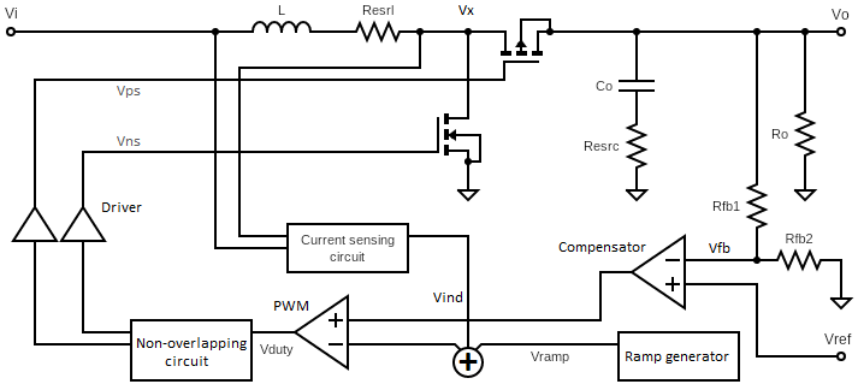
Power management integrated circuits (PMICs) are currently playing a vital role in today's technology [1]. Over the past several years, interest has risen in areas such as artificial intelligence, the internet of things, and electric vehicles. As a result, PMIC are an efficient approach for providing appropriate and stable voltage in practical applications [2]. Recently, switching DC-DC converters has become increasingly popular as an alternative to stacking batteries for boosting purposes [3]. Among these DC-DC converters, boost converters are one type that is widely used in many applications, including green energy [4]–[6].

These DC-DC power converters typically use voltage mode control and current mode control to regulate the output voltage [7], as shown in Figures 1(a) and (b). The compensator generates a compensation voltage V_{ea} by comparing the scaled output voltage of the power stage V_{fb} to the reference voltage V_{ref}. This allows the voltage mode controller to maintain a regulated power stage's output voltage [8]. A sawtooth signal Vramp is generated by a ramp generator circuit, which then goes into a comparator along with the voltage V_{ea}. This causes the comparator to generate a clock signal Vduty to turn the power transistors on and off, which has a proper duty cycle value to compensate for the difference in voltage between the desired voltage and the power converter's output voltage. The current mode is distinct from the voltage mode in that it makes use of a current-sensing loop that passes through the inductor. This feature helps the power

converter to achieve more accurate output voltage regulation and a faster transient response. Subharmonic oscillations may occur if the duty cycle exceeds 50% [9], [10]. In order to address this problem, a few different circuit architectures based on transconductance compensation techniques have been proposed. Nevertheless, adopting these approaches makes circuit design more complicated [11].



(a)



(b)

Figure 1. Control circuits; (a) voltage mode control circuit and (b) current mode control circuit

The performance of a PMIC will change depending on the environment and how it is being used, this will occur regardless of the control system that is being used. The load change on the PMICs will cause the circuit's output voltage to create a transient voltage during a transient time, which is the amount of time required for the output voltage to settle inside the settling band. Figure 2 shows an illustration of transient waveforms. When the load current changes from heavy to light, the output voltage drops by dV1, this transient voltage is referred to as the undershoot. Conversely, when the load current goes from light to heavy, the system output voltage increases by dV2. The term overshoot is used to describe this momentary increase in voltage. dT1 and dT2 denote transient times [12]. Overshoot voltage can lead the circuit to produce a high current, thus burning the chip, while undershoot voltage might result in significant loss of power. Therefore, the transient voltage should not be too low or too high in contrast to the voltage range of the circuit's power supply because doing so would affect the converter's performance. As a result, transient time and transient voltage are important markers of PMICs [13]–[15].

The present research proposes a boost power converter with a pseudo-current hysteresis controller (PCHC) that uses a rail-to-rail current-detecting technique. This converter can be used for applications requiring voltage stepping-up. Because it can rapidly turn on or off the power switches of the power converter using a hysteresis trigger whenever there is a change in the load, hysteresis-controlled technology has the potential to produce a rapid transient response [16], [17]. The organization of the paper is described as: section 2 describes how the proposed architecture would be implemented in circuits, the measurement results are presented in section 3, along with a table comparing the obtained results with previous works, and section 4 gives the conclusions.

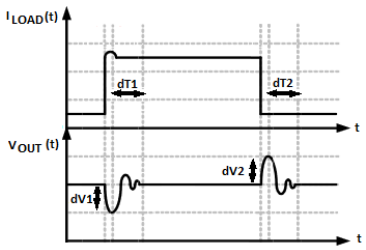


Figure 2. Transient waveforms

2. METHOD

The proposed boost converter, besides the PCHC are illustrated in Figure 3. It is made up of two switching devices in the power stage, as well as a current sensing circuit, a hysteresis voltage controller, a non-overlapping clocks generator circuit, and driving circuits [18], [19]. To create the feedback voltage V_{fb}, the resistors R_{fb1} and R_{fb2} scale the output voltage, which is denoted by V_o, to the reference voltage, which is denoted by V_{ref} [20]. The feedback voltage is expressed as (1):

$$V_{fb} = \left(\frac{R_{fb2}}{R_{fb1}+R_{fb2}}\right) \times V_o \quad (1)$$

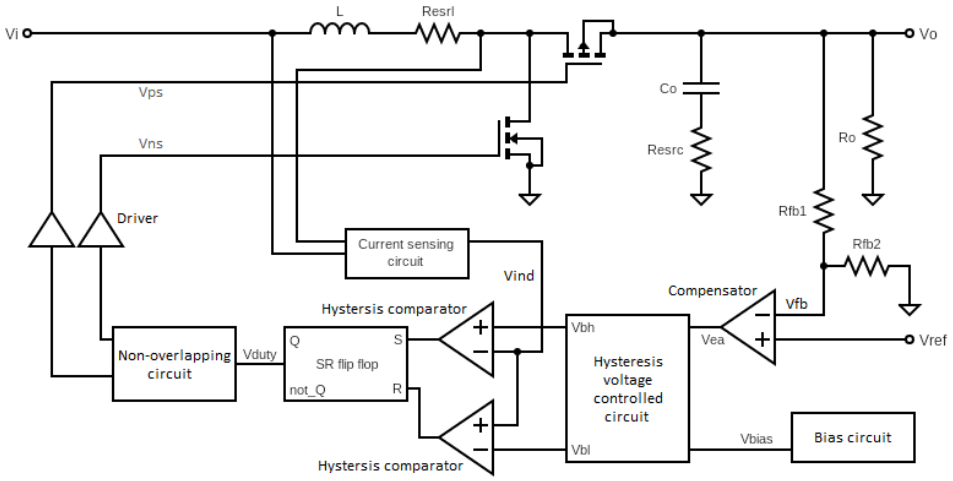


Figure 3. Proposed PCHC boost converter

The compensation voltage denoted by V_{ea} is generated by the compensator, which compares the reference voltage and the feedback voltage. Next, a bias voltage biases the hysteresis voltage-controlled circuit to match the compensation voltage. This is done in addition to controlling the current that flows through the transistor in order to produce the upper and lower limit voltages, denoted by V_{BH} and V_{BL}, respectively.

The current I_c integration with the capacitor C_c forms the sawtooth signal V_{ind}. This ensures that the slope of the sawtooth signal is the same as the inductor current's slope. After that comes the determination of the appropriate duty cycle, which is accomplished by comparing V_{ind} to the limit voltages. Finally, the non-overlapping clocks generator circuit gets the duty cycle signal V_{duty} through a driver to interleave the V_{duty} and separate the two power switches' on-time. Then, the non-overlapping clocks generator circuit controls the power switches through the drivers.

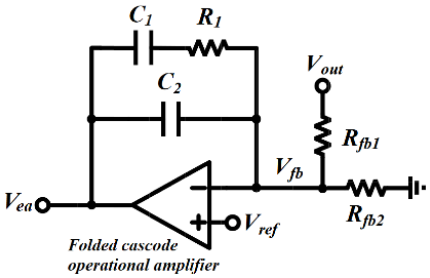
The conventional architecture calls for an additional inductor's current sensing, then the addition of a current-to-voltage converter. The control circuit of the proposed circuit structure sends to the hysteresis-controlled circuit via a capacitor, a voltage signal that is analogous to the inductor current. A current sensor circuit built with a rail-to-rail operational transconductance amplifier (OTA) directly senses the inductor current. This approach has no disadvantages over traditional architecture. Therefore, this sensing method refers to the PCHC method.

2.1. Compensator circuit

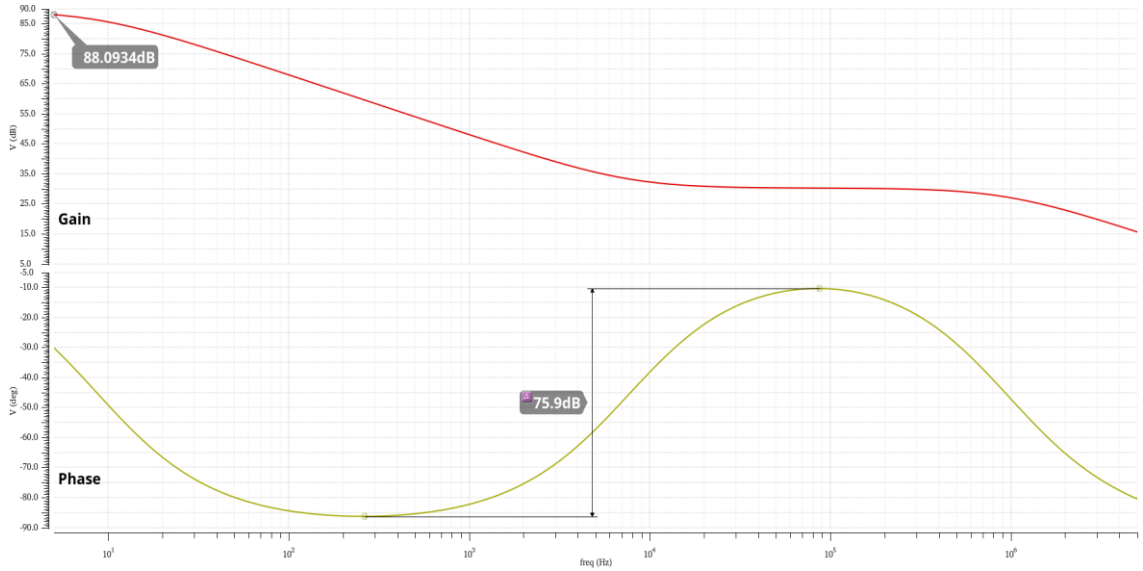
A folded-cascode operational amplifier is integrated with other components, including resistors and capacitors, to form the type II compensator circuit, as shown in Figure 4(a). The compensator circuit is connected to the output voltage feedback path so that the system can be stabilized. In Figure 4(b), the bode plots of the compensation components are illustrated. The high-gain folded-cascode amplifier, which also contributes to the system's stability, improves the closed-loop gain, phase margin, and stability. Two poles and one zero are provided by the type II compensator. The related equations are written as (2) and (3):

$$\left|\frac{V_{ea}}{V_o}\right| = \frac{1+sC_1R_1}{sR_{fb1}(C_1+C_2)+s^2R_{fb1}C_1R_1C_2} \quad (2)$$

$$f_{z1} = \frac{1}{2\pi R_1C_1};\ f_{p1} = \frac{1}{2\pi \times R_1C_1C_2/(C_1+C_2)} \quad (3)$$



(a)



(b)

Figure 4. Type II compensator: (a) circuit and (b) bode plots

2.2. The rail-to-rail current sensing circuit

The rail-to-rail current sensor's key role is to detect the inductor current and send to the control circuitry a voltage signal. As shown in Figure 5(a), this circuit consists of a large input range rail-to-rail OTA, to convert the sensed inductor current to a voltage by a capacitor denoted by C_c. The rail-to-rail amplifier is connected in parallel to the power stage's inductor, specifically between V_i and V_x [21], [22]. The current I_c is generated using the transconductance amplifier's voltage-to-current characteristic. Then, the current I_c is integrated to the capacitor C_c and generates the voltage signal V_{ind} with a slope similar to that of the inductor current. Figure 5(b) presents the waveforms of the current sensing circuit. The voltage V_{ind} is transmitted to the next level's control circuit. By using this architecture, the presented converter's stability and transient response under varying load conditions can be accelerated. Current I_c and voltage V_{ind} can be expressed using (4) and (5):

$$I_c = Gm \times (V_i - V_x) \tag{4}$$

$$V_{ind} = \frac{1}{c_c} \times \int I_c \, dt \tag{5}$$

Figure 5. Rail-to-rail current sensing: (a) circuit and (b) waveforms

2.3. Rail-to-rail operational transconductance amplifier

Rail-to-rail OTA is shown in Figure 6. This circuit improves the input voltage range so that it may replace the current sensing circuit. This would do away with the requirement for additional external resistors to sense the inductor current. An N-type and a P-type OTA form the rail-to-rail OTA. The following describes the circuit's internal structure. Through the current mirrors M_{P7} and M_{N3}, the bias current I_B is supplied to the two OTAs, which is controlled by the bias voltage V_B through M_{P1} and M_B. M_{N1}, M_{N2}, M_{P9}, and M_{P10} transistors have differential input stages. The current on each side of the transistors will be half of I_{MN3} and I_{MP7} due to the designed size symmetry. The N-type OTA combines two current mirrors made up of M_{P2}, M_{P3}, M_{P4}, and M_{P5} to control the output current. The P-type OTA part, like the N-type OTA, regulates the output current with a current mirror built of M_{N6}, M_{N7}, M_{N8}, and M_{N9}. In (6)-(8) can be used to express the circuit's gain. Although this rail-to-rail OTA has less gain compared to a folded-cascode operational amplifier, it has a large bandwidth and consumes less power.

$$Gm_N = gm_N; Gm_P = gm_P \tag{6}$$

$$Z_{out} = \frac{1}{sC_c} \tag{7}$$

$$A_v = Gm \times Z_{out} = \frac{gm_N + gm_P}{sC_c} \tag{8}$$

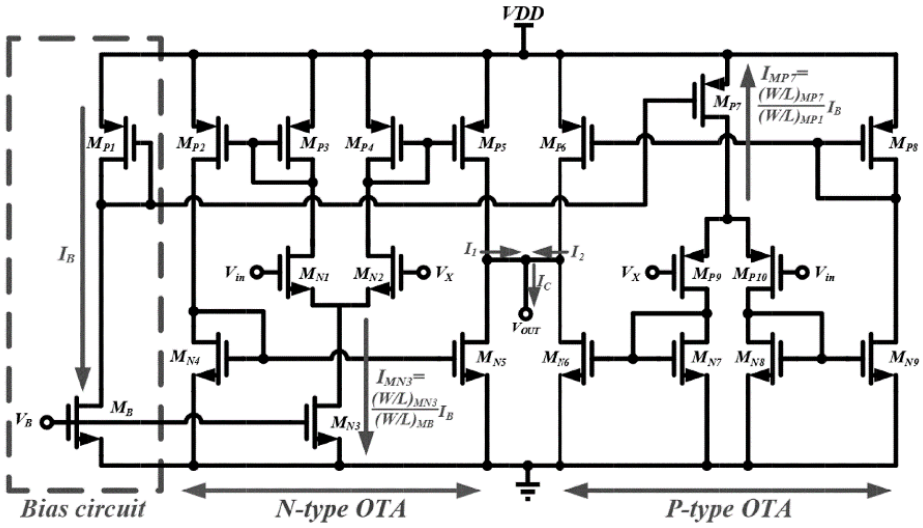


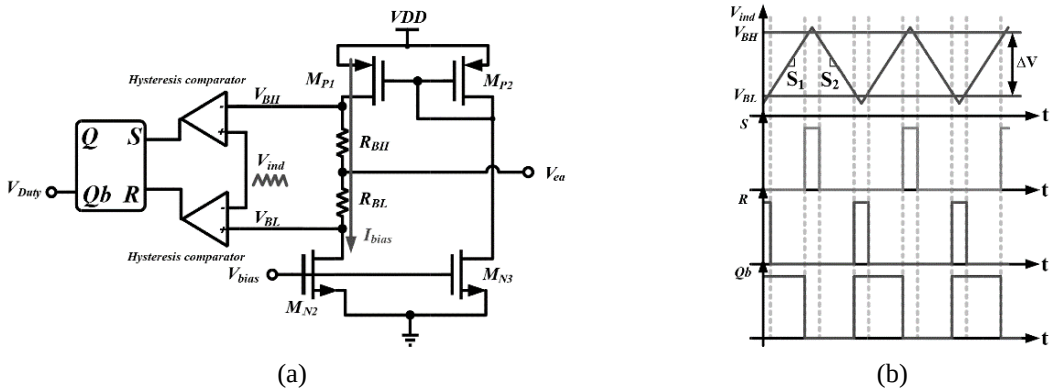
Figure 6. Rail-to-rail OTA circuit

2.4. Hysteresis-controlled circuit

The hysteresis controller architecture is illustrated in Figure 7(a). This circuit controls the current flowing through its transistors through a bias voltage V_{bias} and matches the compensator's output voltage V_{ea}. Resistors R_{BH} and R_{BL} can then form upper and lower limit voltages V_{BH} and V_{BL}, respectively. Then, the limit voltages V_{BH} and V_{BL} are compared to the voltage signal V_{ind} using a hysteresis comparator. The voltage signal V_{ind} is produced by converting the inductor current signal to a voltage signal via a rail-to-rail current sensor. The SR flip-flop gets the comparison signal, which controls the duty cycle. Figure 7(b) illustrates the hysteresis-voltage-controlled circuit's transient waveforms. The hysteresis comparator is represented in Figure 8, which is employed in the hysteresis controller circuit. In (9) and (10) express the associated equations.

$$V_{BH} = V_{ea} + I_{bias} \times R_{BH}; V_{BL} = V_{ea} - I_{bias} \times R_{BL} \quad (9)$$

$$\Delta V = V_{BH} - V_{BL} \quad (10)$$



(a) (b)

Figure 7. Hysteresis-voltage-controlled: (a) circuit and (b) waveforms

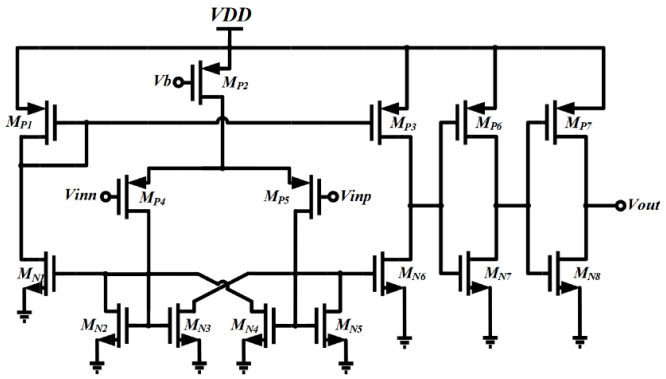
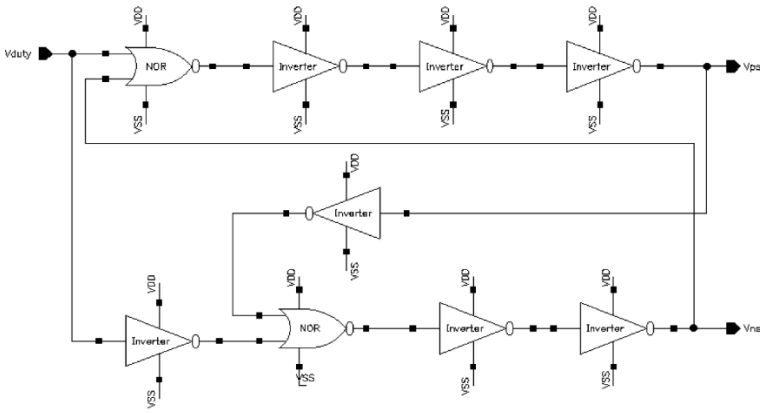


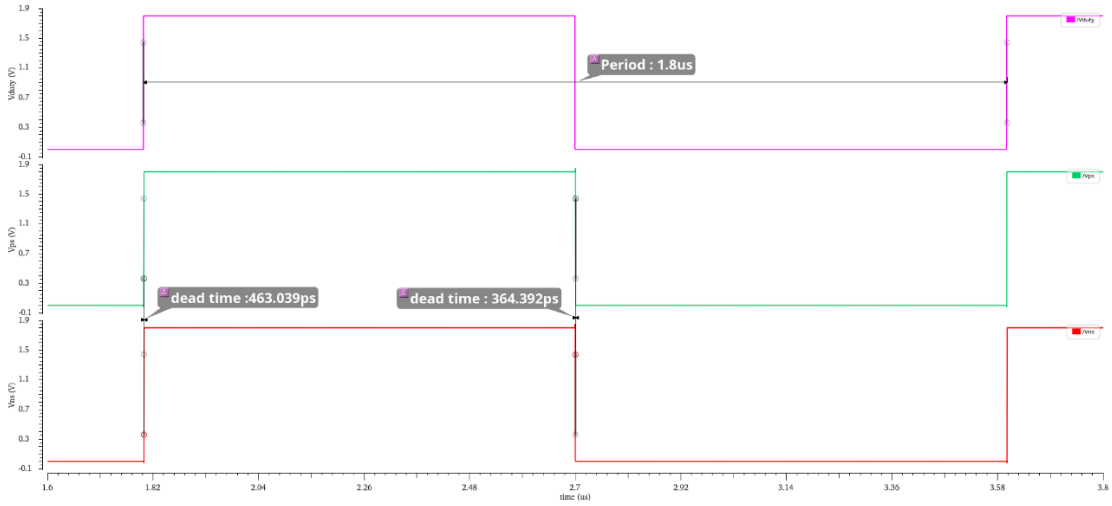
Figure 8. Hysteresis comparator circuit

2.5. Non-overlapping clocks generator circuit

The non-overlapping clocks generator circuit is presented in Figure 9(a). The power transistors of the boost converter, carry a high current. Still, when the P-channel and N-channel power switches are switched on together, they could potentially burn out as the voltage source is short-circuited to the ground [23]. To separate the two power switches' on-times and interleave the V_{duty} produced through the hysteresis controller, the non-overlapping clocks generator circuit is employed. The dead time is adjusted using the delay circuit. It is vital to notice that the dead time should be suitable [24]. The circuit's efficiency may decrease if the dead time is either too short or too long. Finally, the driving circuit produces V_{PS} and V_{NS}, which are then delivered to the power switches to obtain the boost effect. Figure 9(b) represents the dead time timing diagram.



(a)



(b)

Figure 9. Non-overlapping clocks generator: (a) circuit and (b) transient waveforms

2.6. Driver circuit

The switching transistors in the boost converter must handle high currents while also having a low on-resistance. As a result, the size of the switch transistors in the design will be rather large, which leads to a large capacitance at the gate. Therefore, to drive the power switches, a drive circuit made of several inverters is employed [25], as shown in Figure 10.

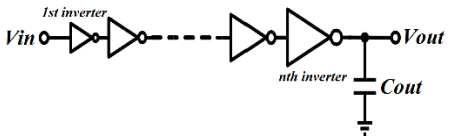
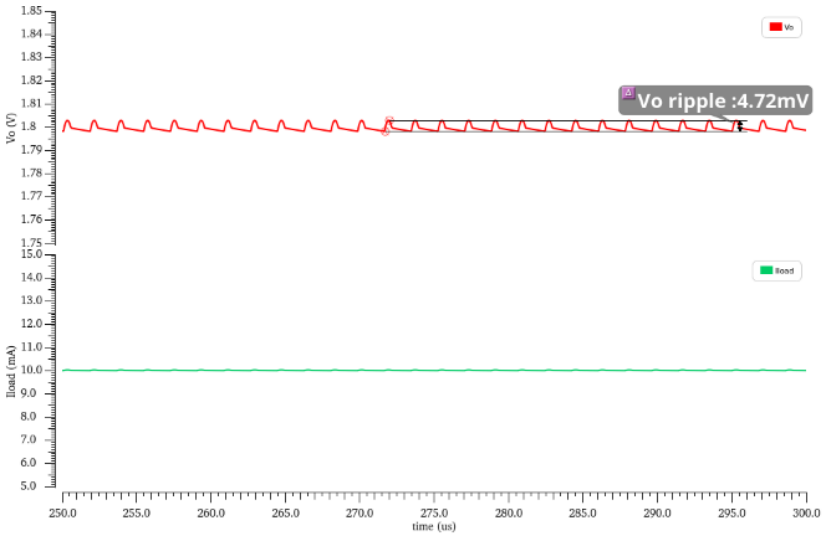


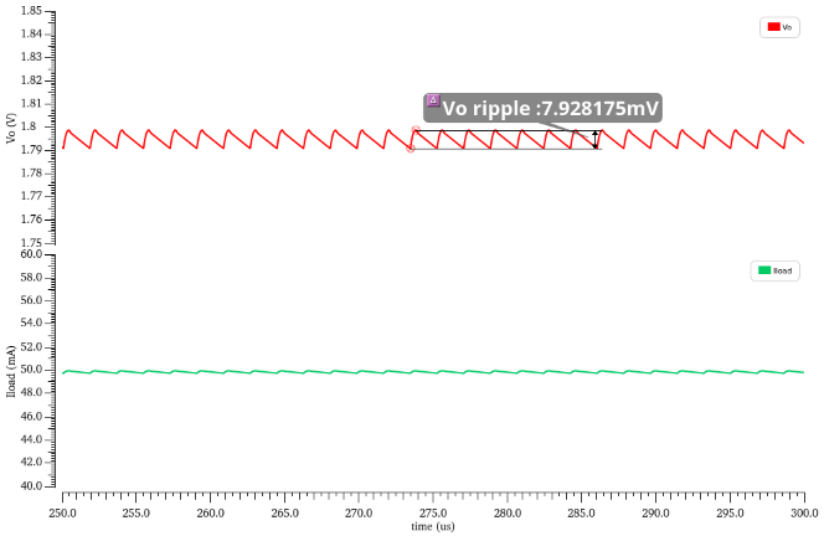
Figure 10. Driver circuit

3. RESULTS AND DISCUSSION

In order to design the proposed boost power converter using PCHC techniques, Taiwan semiconductor manufacturing company (TSMC) 0.18 µm CMOS 1P6M technology was used. The design contains power transistors, a hysteresis-voltage controller, a current detector, a compensation circuit, a non-overlapping clocks generator, and a driving circuit. The transient responses of the power converter's output voltage with load currents of 10 mA, 50 mA, and 100 mA, are presented in Figures 11(a)-(c), respectively. An output voltage of around 1.8 V is generated from an input voltage that ranges from 0.5 V to 1 V.



(a)



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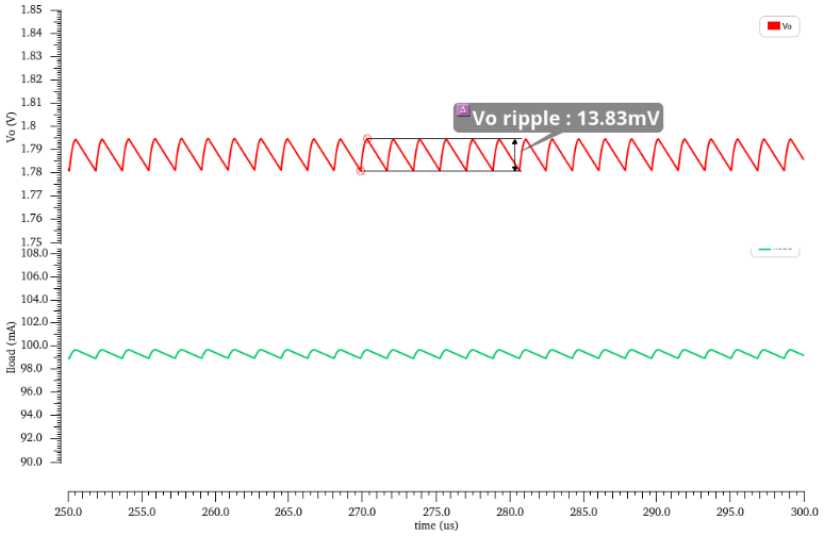
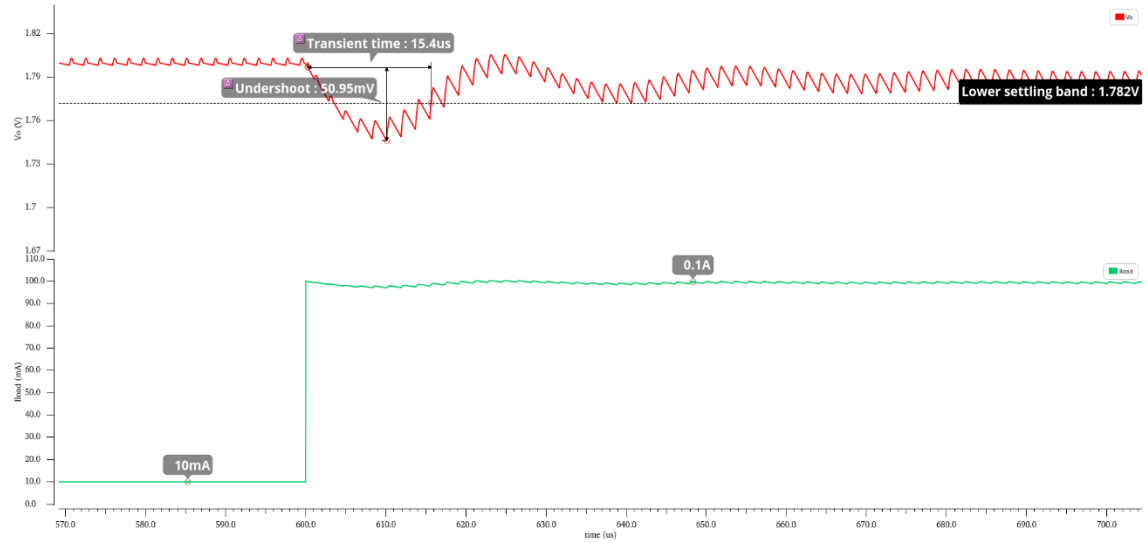


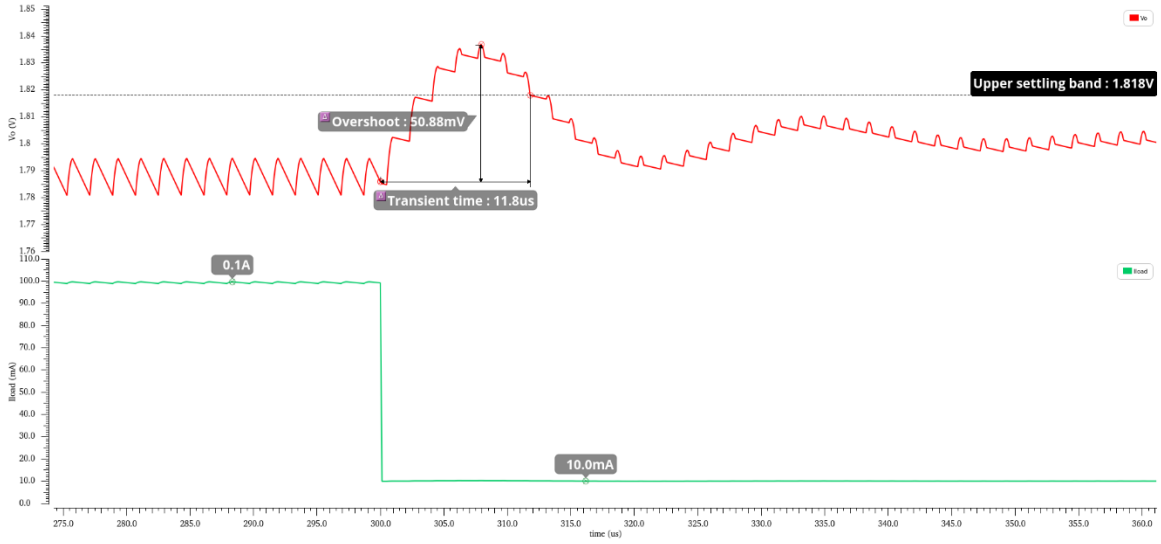
(c)

Figure 11. Measured output voltage V_o with load currents: (a) 10 mA, (b) 50 mA, and (c) 100 mA

The ripple voltage vripple on the power converter's output voltage remains under 14 mV across all load currents. Figures 12(a) and (b) illustrate the transient responses while the V_i is 0.5 V and the V_o is 1.8 V, with load current increasing from 10 mA to 100 mA and decreasing from 100 mA to 10 mA, respectively. The output voltage recovers and remains within the settling band in 15.4 µs after a load current step change from 10 mA to 100 mA, with a 50.95 mV undershoot. Conversely, for a load current step change from 100 mA to 10 mA, the output voltage settles within its settling band in 11.8 µs, with an overshoot of 50.88 mV.



(a)



(b)

Figure 12. Measured output voltage with load current change: (a) 10 mA to 100 mA and (b) 100 mA to 10 mA

Figure 13 represents the measured load regulation, whose load regulation rate is approximately 6.08%/A, the output error voltage is around 9 mV since the load current varies between 10 mA and 100 mA and the output voltage is 1.8 V. Figure 14 represents the obtained power efficiency at various load currents. At 1.8 V output voltage and 10 mA load current, the peak power efficiency is 98.6%. Table 1 summarizes the experimental results of the presented boost power converter with PCHC and compares them to previous works. The proposed boost power converter outperforms other boost power converters, according to the figure of merit (FOM) as expressed in (11):

$$FOM = \frac{Peak\ Efficiency\ (\%) \times Step\ Load\ Change\ (mA)}{Maximum\ Transient\ Voltage (mV) \times Maximum\ Transient\ Response\ (\mu s)} \times 10^{-2} \quad (11)$$

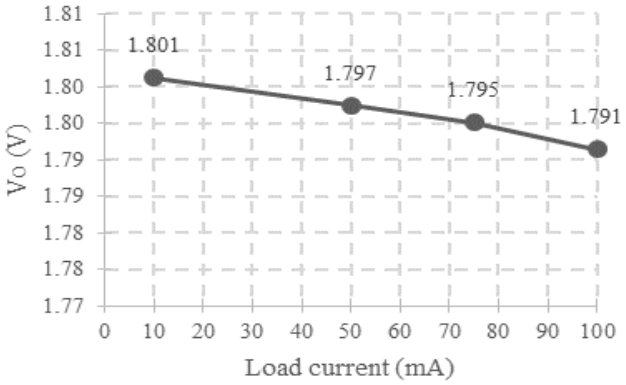


Figure 13. Measured load regulation

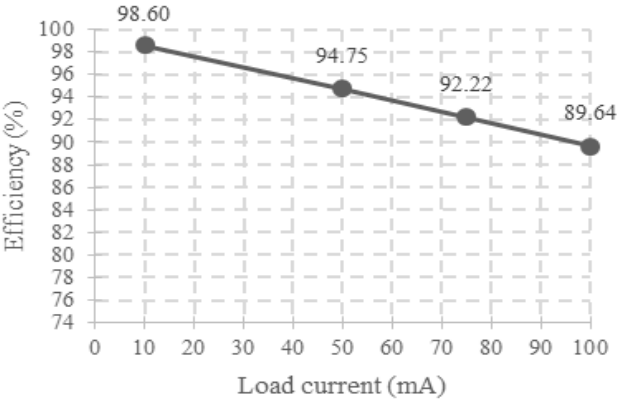


Figure 14. Measured efficiency

Table 1. The performance comparison of the presented boost power converter with previous works

References		[26]	[27]	[28]	This work
Process		0.18 µm CMOS	0.18 µm CMOS	0.18 µm BCD	0.18 µm CMOS
Control technique		KY	AOT	DPU	PCHC
Input voltage range		1.55–1.8 V	0.8–1.4 V	2 –4.2 V	0.5–1 V
Output voltage		2.5 V	1.8 V	3–5 V	1.8 V
Load current range		50–200 mA	10–400 mA	10–200 mA	10–100 mA
Step load change		150 mA	390 mA	400 mA	90 mA
Switching frequency		1 MHz	800 KHz	1 MHz	550 KHz
Inductor		2.2 µH	2.2 µH	4.7 µH	1 µH
Capacitor		4.7 µF	4.7 µF	10 µF	10 µF
Maximum output ripple voltage		10 mV	42.5 mV	15 mV	13.83 mV
Transient response	Light to heavy	24 µs	14 µs	50 µs	15.4 µs
Transient response	Heavy to light	48 µs	46 µs	50 µs	11.8 µs
Transient voltage	Undershoot	90 mV	126 mV	190 mV	51 mV
Transient voltage	Overshoot	105 mV	150 mV	130 mV	51 mV
Peak efficiency		95.7%	92.4%	95.2%	98.6%
FOM		0.02	0.05	0.04	0.11

4. CONCLUSION

An improved boost power converter that has a low transient voltage and a fast transient time has been designed with the use of PCHC techniques in this work. The TSMC 0.18 µm CMOS 1P6M technology was used to design the presented boost power converter. The transient response is significantly improved by further utilizing a PCHC circuit in addition to a rail-to-rail current-detecting circuit. As the load current increases from 10 mA to 100 mA and then back down to 10 mA, the measured transient times are 15.4 µs and 11.8 µs, respectively, and the transient voltages are both 51 mV. The presented boost converter achieves a maximum power efficiency of 98.6% when the load current is set at 10 mA. Overall, the experimental

results, demonstrate that the proposed DC-DC boost converter is effective in achieving the desired output voltage regulation for a range of load currents, with satisfactory efficiency and fast response to changes in load current.

ACKNOWLEDGEMENTS

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